Testing Capacitors' Hard Defects in Notch SC Filters Using the Oscillation Method

Miljana Milić and Vančo Litovski

Abstract - The possibilities for applying the oscillation method to testing Switched Capacitor biquad Notch filter cells with high Quality factor are analyzed in this paper. When applying this method, many surrounding conditions should be met in order to properly test the circuit and to obtain a sustainable and stable oscillations. After solving these problems we have created a fault dictionary that reflects the mapping of hard defects of capacitors into the circuit response. Simulations in LTspice program show that this testing concept is feasible and acceptable for the chosen class of filter cells, especially when we bear in mind all the advantages of the oscillations method.

Keywords – SC filters, Oscillation method, Analogue circuit testing.

I. Introduction

Electronic circuit testing is a very important phase of the electronic circuit design. It requires a lot of time, money, and resources. In order to confirm the correct functioning of the design, one should find the way to check whether the circuit response fits into the definition of the correct functioning [1]. Usually, the main activities in preparation of the testing process, follow two main steps:

1. To establish an input signal (its waveform) which will make the responses of the fault free (FF) and faulty circuit to differ, and
2. Among all such signals, to choose the one that enables fastest and cheapest testing.

Only the correct designs can qualify for the correct project. One of the important aspects of the circuit design is the implementation of a concept Design for Testability (DFT). Second, more important aspect, is the test signal synthesis. A designer here gets a task to generate signal that will be applied to the inputs of the circuit to be tested DUT (Device Under Test), as well as to create a list of the required FF responses which will be compared with those obtained during the DUT testing.

At the other hand, problems that occur during analogue circuit testing are numerous. They arise from the lack of accessible internal circuit nodes, nonlinearities in the circuit, presences of different noises, parameters' variations and others [2].

An important tool that helps solving many of these problems is the fault simulator. In order to successfully prepare a test for a particular DUT, it is necessary to define the set of most probable defects, to describe their models and to embed them into the circuit description. The final result of this procedure should be a Fault dictionary, which can later be used for both testing and diagnostics [3], [4].

One of the crucial types of electronic devices are filters. They are inevitable part of every modern electronic system. Having in mind the requirements for the small circuit size, ability of integration on a chip, and reduction of the design costs, the best solution for the analog filter implementation is the SC technique.

The circuit realized using capacitors, resistors, and operational amplifiers have many drawbacks such as large components tolerances, which can affect the accuracy of the functions that should be performed. On the other side, the accuracy of the SC realized circuits is determined by the accuracy of the capacitances' ratio in it. SC technique represents a very smart application of the switching at the small capacitances on the chip, in order to get the same behaviour and functionalities as large resistors in an MOS integrated circuit. These resistors would, in non SC technique, occupy large chip areas [5], [6].

The main advantages of the SC technique are [7]:

- compatibility with the standard CMOS technology,
- high timing constant accuracy,
- good linearity,
- good temperature characteristics.

Its disadvantages are:

- bad influence of the clock signal,
- the requirement for non-overlapping clock signals,
- bandwidth limitation due to the use of non-overlapping clock.

One possible solution of the problem with SC filters testing, is the oscillation method. By applying this method, a filter to be tested is converted into an oscillator, by establishing a positive feedback [2], [8]. Doubts about using the frequency dimain analysis or time domain analysis are avoided here. Since we have a filter cell, the most proper analysis domain would consequently be the frequency domain [1]. That, however, would impose a number of new doubts about the frequency, amplitude and phase of the test signal. Similarly, the analysis in a time domain also throws a bunch of questions regarding the shape of the input test signal [1].

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When oscillation method testing concept is used, there is no need to perform test signals sinthesys, since an oscillator only needs a power supply to maintain stabile oscillations. A special feature of the OBT is that it covers all defects in the circuit. Namely, in the structural test synthesis, it is necessary to generate one test signal for each potential defect of the circuit. With the OBT, it is expected that effects of all potential defects influence the oscillators output signal. This dramatically reduces the test engineers' work.

Since during the OBT, only one signal is observed, that is the output filter/oscillator signal, the observability is always guarantied. Filter's output is always accessible, and by observing it one can conclude if the circuit oscillate and at what frequency.

During the theoretical introduction and the development of the OBT [5], [6], as well as during its development and application to the SC filters [8], [9], one fact was constantly being ignored. Namely, the oscillation frequency of the obtained testing oscillator is normally above the operational amplifier`s (embedded in the filter) cut-off frequency (3dB). It was by default assumed that the opamps have an infinite gain, while its phase shift is neglected. It was shown, however, that these approximations are not justified and the theoretical data (oscillation frequency) obtained in that way are not realistic [10].

In the following sections principles of the oscillation testing method will be described first. After that, it will be explained in more detail the functionality and the implementation of the active SC Notch filter with a high Quality factor. Principles of its testing will then be further analyzed. Application of the OBT was verified by simulation in LTspice environment. The aim of the research was to establish the OBT environment for the CUT. As the result, we have obtained stable oscillations of the output signal, and then the circuit was tested for presence of catastrophic defects in capacitors. With the result of the defects modelling and simulation, we have obtained a Fault dictionary which is shown in the last sections of the paper, where experimental results and conclusions are given.

II. Oscillation Based Testing

The idea of using astable behaviour of the circuit with a positive feedback is not so old [8]. The first step in its implementation is to transform CUT into an oscillator. By measuring the oscillation frequency, one can determine whether the circuit is faulty or fault free.

In this way CUT is transformed into a signal generator. The main advantage of such an approach is that no input signal is required. Instead, observing only a few periods of obtained output signal is enough to determine their duration. In general, this method is applicable to analogue and mixed circuits, and in its first step involves the decomposition of the complex system under test (SUT), to simpler blocks that can be tested separately [9]. Fig. 1 shows the basic building blocks for the OBT technique. During the second, testing phase, particular blocks under test (BUT-s) are converted into oscillators. The third phase of OBT involves measuring their oscillation frequences, and their comparison to the FF topology measurement results, in the final phase.

The obtained signal waveforms should now be analysed, which usually involves frequency measurements, but can also include the DC value measurement and analysis of the harmonic distortions. Since the obtained signals are somehow standardized (sinusoidal shapes or the arrays of pulses), these analysis can be standardized regardless of the block to be tested [2].

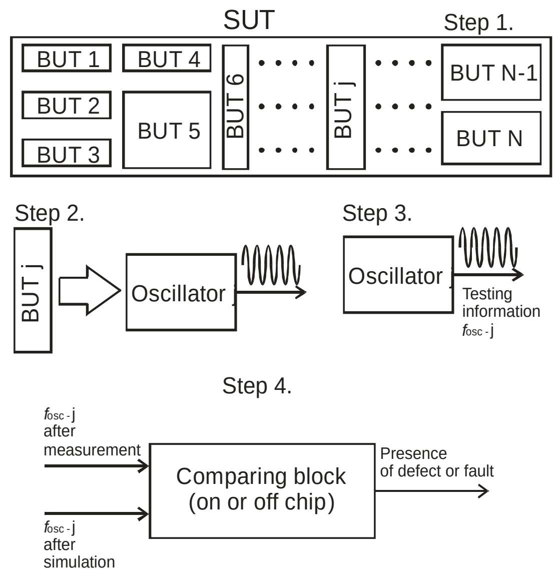

Fig. 1. The illustration of the OBT technique

Although looking simple at the first site, the implementation of this method is limited by the possibility to convert the nominal circuit into an oscillator, where the presence of the defect reflects the oscillation frequency. This process is difficult to systematize, and depends solely on the experience and the creativity of the designer. Principles of oscillator design cannot easily be applied for the OBT implementation. Goals of designing OBT oscillators are not stable frequency and amplitude of the generated sinusoidal signal, but they are created so that the amplitude and frequency of oscillation (not necessarily proper sinusoid) be as sensitive as possible to the presence of defects in the circuit, whatever nature they were.

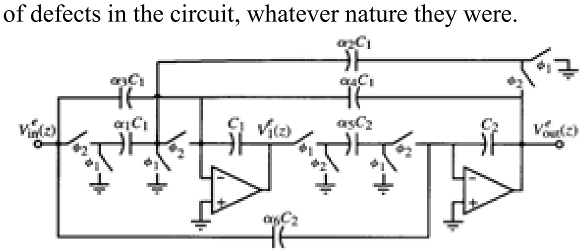

Fig. 2. High Q Biquad Notch SC filter cell

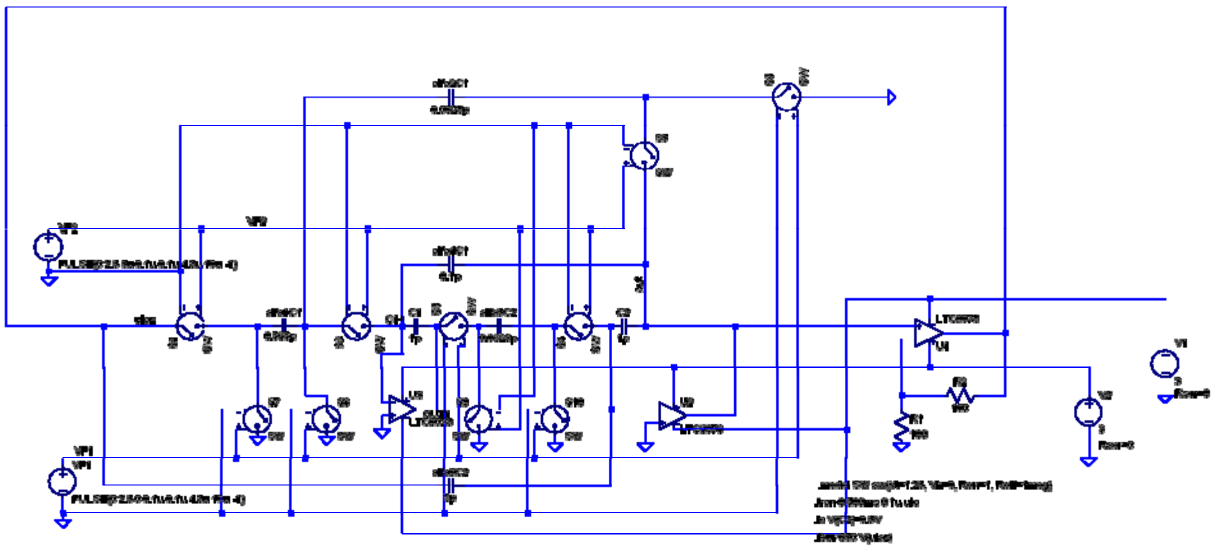

Fig. 3. The Biquad Notch SC filter with high Q factor in LTspice

In order to cover all defects with the test, it is sometimes necessary to include some other measurements (for example of the supply current in CMOS circuits), or analyze some other parameter of the response.

III. Active SC Notch Filter Cell with High Quality Factor

Fig. 2 shows the topology of the universal second order SC filter cell. This topology has the ability of coefficient modification, that is capacitors' variation in order to realize all four types of signal filtering: HP, LP, BP, and BS.

With a proper choice of the coefficients the realized circuit performs Notch, that is Band Stop filtering of the input signal [11]. In our particular case the filter's specifications are: central cut-off frequency f_0=1kHz, and quality factor Q=10. Beside this, we must choose the frequency of the two-phase, non-overlaping clock signal to be 100kHz, and capacitances C_1 and C_2 to have values of 1pF. The filter's transfer function can be represented as (1):

$$T(s)=\frac{V_{out}(s)}{V_{in}(s)}=-\frac{K_2s^2+K_1s+K_0}{s^2+\frac{\omega_0}{Q}s+\omega_0^2}. \tag{1}$$

Coefficients that determine values of capacitances are calculated according to equations (2-6):

$$\alpha_1=\frac{K_0T}{\omega_0} \tag{2}$$

$$\alpha_2=|\alpha_5|=\omega_0T \tag{3}$$

$$\alpha_3=\frac{K_1}{\omega_0} \tag{4}$$

$$\alpha_4=\frac{1}{Q} \tag{5}$$

$$\alpha_5=K_2. \tag{6}$$

In order to implement Notch filtering, one should choose K_1=K_2=0, and K_0=$(3\cdot\omega_0)^2$. The frequency response of such a filter cell is shown in Fig. 4. The notch frequency, as seen from this figure is 1kHz.

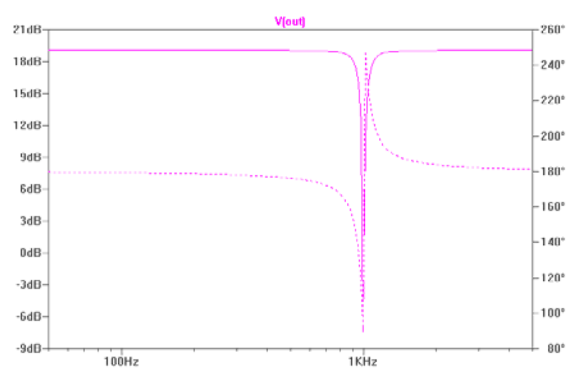

Fig. 4. Frequency response of the filter. The full line is the amplitude, and the doted is the phase characteristic.

LTspice shematics [12] of filter's implementation, after it is transformed into an oscillator, is presented in Fig. 3. The switches are modeled to have open resistance of 1MΩ, and closed 1Ω. For this purpose LTC6078 opamps are used from the LTspice CMOS library.

IV. OBT Notch Testing

In order to apply the OBT method to Notch filter testing, the oscillator output signal first have to be

TABLE I
FAULTS DICTIONARY

Defect number	Defects	f_{osc} [kHz]	Amplitude [dB]	Phase [degrees]
0	FF	654	-19.78	-130.37
1.	α_2 C_1 - open	636	-22.51	-171.56
2.	α_2 C_1 - short	49.87	-72.33	55.61
3.	α_4 C_1 - open	654	-22.48	177.34
4.	α_4 C_1 - close	0.969	-48.87	-167.34
5.	α_1 C_1 - open	653.46	-19.43	-82.35
6.	α_1 C_1 - close	2.298	-29.33	-159.05
7.	C_1 - open	1.2	-23.63	-154.27
8.	C_1 - close	16.85	-75.70	88.98
9.	α_5 C_2 - open	87.06	-65.22	29.74
10.	α_5 C_2 - close	No oscillations	3V DC	
11.	C_2 - open	654	-18.61	-150.44
12.	C_2 - close	29.12	-67.65	137.84
13.	α_6 C_2 - open	2.22	-5.55	-50.28
14.	α_6 C_2 - close	21.90	-10.08	121.96

amplified and stabilized, before it is brought back to the circuit's input. This is shown in Fig. 3. An additional amplifying stage is introduced in the feedback loop. The gain of the additional amplifier is 2, and the achieved voltage levels are ±300mV. When we deal with the FF filter, its oscillation frequency is 654Hz. Very high influence of all opamps' nonidealities can be noticed here. Namely, in case of using ideal opamps, oscillations would occur at the notch frequency of the filter that is 1kHz [10].

When defects are inserted, tree situations can happen: oscillation at the frequency of the FF circuit, change of the oscillation frequency in compare with the FF circuit, and the apsence of the oscillations. In the first case, presence of the defect cannot be detected by only observing the oscillation frequency, and some additional measurement or output signal parameter analysis is required (for example, harmonic distorsion, DC value or phase etc.). In the second and third case, presence of defects in the circuit is much easier to detect.

Fault simulation has key role during the test synthesis. For the Notch SC BS filter, it is recomended to use some analog circuit simulator. Unfortunately, too large number of different circuit simulators use stable numerical integration formulae in solving differential equations in the time domain, such as the Euler's backward rule, or some group of higher order rules such as Gear's formulae are [10], [13]. With a stable approximation rule one cannot simulate an astable circuit, such the oscillator is [14], [15]. Because of this limitation, we have chosen to use LTspice simulator, since it offers trapezoid and modified trapezoid rule for the time derivative approximation.

Fault simulations

There are two groups of defects in analog circuits: hard that is chatastrophic, that change the circuit topology, and soft, that is, parametric, that affect just some parameter value within the circuit. During the testing and OBT oscillator simulation, hard defects of the capacitances were checked. The aim of this research is to create the OBT enviroment that will ensure stable oscillations. By simulating the chatastrophic defects, we have proven the theoretical assumptions about the effects of the defects to the oscillation frequency of the OBT and to additional parameters of the circuit's response.

Prior to the simulation it is necessary to set the initial conditions in order to enable the circuit to oscillate.

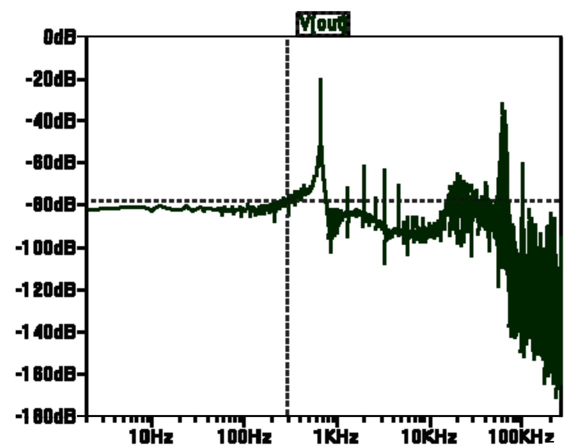

Fig. 5. FFT analysis of the FF circuit

Table I shows the simulation results for hard defects. It gives the oscillation frequencies in the absence and in the presence of the particular capacitance defects. First row corresponds to the FF response analysis, while others refer to capacitances' hard defects. It can be noticed that in some cases of the hard defects, the oscillation frequency is very similar to the FF one. If we only observe this parameter, some defects in this case, can be pronounced unrecognizable. This points to the fact that some other response parameter should be measured and observed too.

Table I also gives some important parameters of the output signal FFT analysis. We have chosen to observe the amplitude and the phase of the output signals using its spectre, which are obtained after the FFT analysis. The spectre of the output signal for the FF circuit is shown in Fig. 5.

Additional results indicate that these parameters of the circuit's response can be used during testing not only for rejecting bad devices, but for diagnostics and recognition of the particular defects in the circuit, too [16], [17].

V. CONCLUSION

In this paper we have shown an efficient implementation of the OBT method for testing active SC Notch biquad filter cells. By measuring the oscillation frequency and observing the amplitude and phase of the first harmonic for the output signal, we have achieved 100% defect coverage. In this study we took into account the influence of the real parameters of the opamp model. The applied testing method does not require development and application of any input test signal, and all measurements are performed for only one signal at only one test-point. By applying additional simple logic, this technique can be efficiently used as part of some BIST, Analogue Scan or DFD solution. Future research will be directed to analysis of effects of switching defects; hard and soft/ideal or real.

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